METHOD OF OPERATING DYNAMIC RANDOM ACCESS MEMORY

DESCRIPTION

CROSS-REFERENCE TO RELATED APPLICATION

[Para 1]   This application claims the priority benefit of Taiwan application serial no. 93119966, filed July 2, 2004.

BACKGROUND OF THE INVENTION

[Para 2]   Field of the Invention

[Para 3]   The present invention relates to a method of operating a dynamic random access memory (DRAM), and more particularly to a method of operating a DRAM without using a charge pump.

[Para 4]   Description of Related Art

[Para 5]   Dynamic random access memory (DRAM) has been widely used in a variety of electronic products, such as computers, memory cards or related products. FIG. 1 is a schematic drawing showing a prior art memory cell array of DRAM. In the prior art design, a memory cell comprises a switch device 100 and a charge storage device 110. The charge storage device 110 is coupled to the bit line BL or the bit line bar BLB via the switch device 100. The switch device 100 is either a P-type or an N-type metal oxide semiconductor (MOS) device and can be controlled via the voltage of the word lines WL0-WL3.

[Para 6]   In the conventional operating method of DRAM, the voltage at the point (called memory point thereafter) 120 represents the data stored in the memory cell where the charge storage device 110 is coupled to the switch device 100 at the memory point 120. Generally, when the data is logic 0, the voltage of the memory point 120 is pulled down to zero voltage. When the data is logic 1, the voltage of the memory point 120 is pulled up to the power voltage VDD. During the reading operation, the bit line BL and the bit line bar BLB are charged to the same voltage, e.g. one half of the power voltage VDD. In order to turn on the switch device 100, the word line WL0 is charged to the voltage VPP, which is about VDD+VTN+0.3V, wherein VTN represents the threshold voltage of the switch device 100. After the switch device 100 is turned on, the voltage of the bit line BL is changed because voltage is being shared with the charge storage device 110 hence the sensor of DRAM senses the voltages of the bit line BL and the bit line bar BLB. The data stored in the memory cell can then be identified by the voltage differences.

[Para 7]   FIG. 2 is a circuit block diagram showing a prior art driving circuit of DRAM. The operation of the DRAM 20 is similar to that described above. However, there is a disadvantage in the prior art DRAM. In order to provide the voltage VPP, which is higher than the normal power voltage, a charge pump 200 is applied in the driving circuit of the DRAM shown in FIG. 2. Since the bit line BL and the bit line bar BLB have to be charged to one half of the power voltage VDD, DRAM 20 has to supply direct current of VDD/2. Because the charge pump 200 and the additional direct current, the DRAM 20 consumes powers even when it is in stand-by mode. The power consumption shortens the service life of cells of portable devices.

SUMMARY OF THE INVENTION

[Para 8]   Accordingly, the present invention is directed to a method of operating dynamic random access memory (DRAM). The method is capable of operating DRAM without using a charge pump and a VDD/2 voltage.

[Para 9]   The present invention is directed to a writing operation of DRAM. The writing operation writes data in the DRAM without using a charge pump.

[Para 10]   The present invention is directed to a reading operation of DRAM. The reading operation reads data stored in the DRAM without using a charge pump.

[Para 11]   According to an embodiment of the present invention, the method is adapted to the DRAM using a word line and a word line bar, and a charge storage device is adapted for storing data. The charge storage device is coupled to the word line via a switch device. When the switch device is turned on, a switch voltage drop is generated between two ends of the switch. The charge storage device is programmed with a first voltage, which is VDD minuses the switch voltage, or a zero voltage. The method can also access the data. For accessing the data, the word line and word line bar are charged to the power voltage. Next, the switch device is turned on and then the data stored in the charge storage device is determined according to a voltage difference between bit line and bit line bar.

[Para 12]   According to another embodiment of the present invention, a voltage of the bit line bar is pulled down a preset voltage before determining the data stored in the charge storage device. The preset voltage is one half of the voltage drop on the bit line while the switch device is being turned on after the charge storage device is being programmed by a zero voltage.

[Para 13]   Accordingly, the DRAM can be operated with the power voltage without using a charge pump.

[Para 14]   The above and other features of the present invention will be better understood from the following detailed description of the preferred embodiments of the invention that is provided in communication with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[Para 15] FIG. 1 is a schematic drawing showing a prior art memory cell array of DRAM.

[Para 16] FIG. 2 is a circuit block diagram showing a prior art driving circuit of DRAM.

[Para 17] FIG. 3 is a circuit block diagram showing a circuit layout of a dynamic random access memory (DRAM) according to an embodiment of the present invention.

[Para 18] FIG. 4 is a control line/data line time sequence of a writing operation of a DRAM according to an embodiment of the present invention.

[Para 19] FIG. 5 is a control line/data line time sequence of a reading operation of a DRAM according to an embodiment of the present invention.

DESCRIPTION OF EMBODIMENTS

[Para 20] FIG. 3 is a circuit block diagram showing a circuit layout of a dynamic random access memory (DRAM) according to an embodiment of the present invention. The design of memory cells is shown in FIG. 1. In this embodiment, most of the devices are similar to those shown in FIG. 2 except that the DRAM 30 of this embodiment does not require the charge pump 200. In this embodiment, the memory array 310 uses the VDD applied from a power terminal (not shown) as the maximum voltage. Generally, the voltage applied for storing logic 1 data can be slightly lower than the power voltage VDD; and the voltage applied for storing logic 0 data can be a zero voltage and vice versa. The maximum voltage applied to the bit line BL and the bit line bar BLB is the power voltage VDD as shown in FIG. 1.

[Para 21] The present invention is also directed to a method of operating the DRAM without using a charge pump. The method could be employed on the DRAM shown in FIG. 2 or FIG. 3. FIG. 4 is a control line/data line time sequence of a writing operation of a DRAM according to an embodiment of the present invention.

[Para 22] Following are the descriptions of writing logic 0 data in memory cells. For writing data in memory cells, the voltage of the word line WL0 is pulled up to the power voltage VDD provided by the power terminal for turning on the switch devices of the memory cells. The data input signal DATA_IN is written as logic 0. After the voltage of the word line WL0 is pulled up to the power voltage VDD, data is transmitted to the bit line BL. By turning on the switch device, the data is written into the memory cell. After the logic 0 is written into the memory cell, the storage voltage VSN of the memory cell becomes zero.

[Para 23] The method of writing logic 1 is similar to that of writing logic 0 except that the storage voltage of the memory cell is VDD negative VTN, wherein VTN represents the voltage drop in the switch device (hereinafter, switch voltage drop). One of ordinary skill in the art will understand that the zero voltage may represent logic 1, and the voltage VDD–VTN may represent logic 0 depending on the design of the circuit.

[Para 24] The present invention is also directed to a reading operation of DRAM. FIG. 5 is a control line/data line time sequence of a reading operation of a DRAM according to an embodiment of the present invention. In this embodiment, according to the arrangement of the word lines WL0–WL3, the data stored in the memory cells are 0, 1, 0 and 1. In this embodiment, the sequence of the reading operation follows WL0, WL1, WL2 and WL3. The word lines WL0–WL3 and the bit line BL and the bit line bar BLB are coupled as shown in FIG. 1. Signals PULL_BL and PULL_BLB control pulling down the voltage of the bit line BL and the bit line bar BLB. In this operation, logic low is the active standard.

[Para 25] In this embodiment, the bit line BL and the bit line bar BLB are charged to the power voltage VDD. The word line WL0 is then charged to the

power voltage VDD. Due to the charging of the word line WL0, the switch device of the memory cell is turned on. When the switch device is turned on, the logic 0 data stored in the memory cell is coupled to the bit line BL, and the power voltage VDD of the bit line BL is pulled down. The pull-down voltage of the bit line BL caused by the logic 0 data is called a logic 0 read pull-down voltage. After the word line WL0 turns on the switch device, the voltage of the bit line bar BLB is pulled down before the sensor is activated, i.e. the pull-up to logic high of SA ACTIVE. The pull-down voltage is preferably one half of the logic 0 read pull-down voltage. Accordingly, while the switch device is being activated, the sensor can easily sense the voltage difference between the bit line BL and the bit line bar BLB so as to sense that the data stored in the memory cell is logic 0. After the sensing step is completed, the voltage of the bit line is pulled down to logic 0 so as to rewrite data into the memory cell.

[Para 26] One of ordinary skill in the art will understand that the pull-down voltage of the bit line bar BLB is modifiable. As long as the differential voltage between the bit line BL and the bit line bar BLB can be sensed, the operation of the DRAM can be performed. The present invention, therefore, is not limited to this embodiment.

[Para 27] The step of reading the logic 1 data stored in the memory cell coupled to the word line WL1 is similar to that of reading the logic 0 data except that the memory cell controlled by the word line WL1 is coupled to the bit line bar BLB. The logic 1 data is represented by a zero voltage. The operations of the bit line BL and the bit line bar BLB in this embodiment are reverse to those of reading the data stored in the memory cell coupled to the word line WL0. The operations of the control lines PULL_BL and PULL_BLB are also reverse to those of reading the data stored in the memory cell coupled to the word line WL0.

[Para 28] Following are the descriptions of operations of the control line/data line for reading the logic 0 data. Referring to FIG. 5, the data stored in the memory cell controlled by the word line WL 2 is logic 0. After the bit line BL and the bit line bar BLB are charged to the power voltage VDD, the word line WL2 turns on the switch. As the memory cell is coupled to the bit line bar BLB,

the voltage of the logic 0 is preferably VDD-VTN. The memory cell stores the logic 0 data. The turning-on of the memory therefore does not affect the voltage of the bit line bar BLB. After the reading process, the bit line bar BLB is maintained at higher voltage for rewriting the data into the memory cell. With the condition similar to that described above, when reading the data stored in the memory cell controlled by the word line WL3, the operations of the control line/data line are similar to those of reading the data stored in the memory cell coupled to the word line WL2 except that the voltages are applied to the bit line BL, the bit line bar BLB and the control lines PULL_BL and PULL_BLB.

[Para 29] According to an embodiment of the present invention, the maximum voltage is the power voltage VDD provided by the power terminal without using the charge pump. The bit line BL and the bit line bar BLB need not be maintained at the voltages, such as the transient voltage resulting from sharing the voltage with the memory cell or the transient pull-down voltage, except for the power voltage VDD and the ground voltage GND. During stand-by mode, no additional direct current is required to maintain the voltages of the bit line BL and the bit line bar BLB. Therefore, the operating method of the DRAM of the present invention consume less power.

[Para 30] Although the present invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be constructed broadly to include other variants and embodiments of the invention, which may be made by those skilled in the field of this art without departing from the scope and range of equivalents of the invention.